## CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor device, comprising:

forming a ferroelectric capacitor in a capacitor layer above a semiconductor body; and

forming a hydrogen barrier above the ferroelectric capacitor, wherein the hydrogen barrier comprises silicon rich silicon oxide or amorphous silicon.

2. The method of claim 1, wherein forming the hydrogen barrier comprises:

forming a first hydrogen barrier layer over the ferroelectric capacitor; and

forming a second hydrogen barrier layer above the first hydrogen barrier layer, the second hydrogen barrier layer comprising silicon rich silicon oxide or amorphous silicon.

3. The method of claim 2, wherein the first hydrogen barrier layer comprises a material that does not react with a ferroelectric material of the ferroelectric capacitor.

4. The method of claim 3, wherein the first hydrogen barrier layer comprises aluminum oxide.

5. The method of claim 4, wherein the second hydrogen barrier layer comprises silicon rich silicon oxide.

6. The method of claim 2, wherein the second hydrogen barrier layer comprises amorphous silicon.

7. The method of claim 2, wherein forming the second hydrogen barrier layer comprises forming silicon rich silicon oxide over the first hydrogen barrier layer, and wherein forming the hydrogen barrier further comprises:

forming a third hydrogen barrier layer over the second hydrogen barrier layer, the third hydrogen barrier layer comprising amorphous silicon; and

forming a fourth hydrogen barrier layer over the third hydrogen barrier layer, the fourth hydrogen barrier layer comprising silicon rich silicon oxide.

8. The method of claim 2, wherein the second hydrogen barrier layer comprises silicon rich silicon oxide, and wherein the second hydrogen barrier layer is an inter-level dielectric.

9. A method of fabricating a semiconductor device, comprising:

forming a ferroelectric capacitor in a capacitor layer above a semiconductor body; and

forming a multilayer hydrogen barrier above the ferroelectric capacitor, wherein the hydrogen barrier comprises at least one silicon rich silicon oxide layer.

10. The method of claim 9, wherein forming the multilayer hydrogen barrier comprises forming at least one aluminum oxide layer above the ferroelectric capacitor.

11. The method of claim 9, wherein forming the multilayer hydrogen barrier comprises forming a silicon rich silicon oxide inter-level dielectric above the ferroelectric capacitor.

12. The method of claim 9, wherein forming the multilayer hydrogen barrier comprises forming at least one amorphous silicon layer above the ferroelectric capacitor.

13. The method of claim 9, wherein forming the multilayer hydrogen barrier comprises:

forming an aluminum oxide layer over the ferroelectric capacitor; and

forming a first silicon rich silicon oxide layer over the aluminum oxide layer.

14. The method of claim 13, wherein forming the multilayer hydrogen barrier further comprises forming an amorphous silicon layer over the first silicon rich silicon oxide layer and forming a second silicon rich silicon oxide layer over the aluminum oxide layer.

15. A semiconductor device, comprising:

a ferroelectric capacitor formed in a capacitor layer above a semiconductor body; and

a hydrogen barrier above the ferroelectric capacitor, the hydrogen barrier comprising silicon rich silicon oxide or amorphous silicon.

16. The semiconductor device of claim 15, wherein the hydrogen barrier comprises:

a first hydrogen barrier layer formed over the ferroelectric capacitor; and

a second hydrogen barrier layer formed above the first hydrogen barrier layer, the second hydrogen barrier layer comprising silicon rich silicon oxide or amorphous silicon.

17. The semiconductor device of claim 16, wherein the first hydrogen barrier layer comprises a material that does not react with a ferroelectric material of the ferroelectric capacitor.

18. The semiconductor device of claim 17, wherein the first hydrogen barrier layer comprises aluminum oxide.

19. The semiconductor device of claim 18, wherein the second hydrogen barrier layer comprises silicon rich silicon oxide.

20. The semiconductor device of claim 16, wherein the second hydrogen barrier layer comprises amorphous silicon.

21. The semiconductor device of claim 16, wherein the second hydrogen barrier layer comprises silicon rich silicon oxide, and wherein the hydrogen barrier further comprises:

a third hydrogen barrier layer formed over the second hydrogen barrier layer, the third hydrogen barrier layer comprising amorphous silicon; and

a fourth hydrogen barrier layer formed over the third hydrogen barrier layer, the fourth hydrogen barrier layer comprising silicon rich silicon oxide.

22. The semiconductor device of claim 16, wherein the second hydrogen barrier layer comprises silicon rich silicon oxide, and wherein the second hydrogen barrier layer is an inter-level dielectric.

23. A semiconductor device, comprising:

a ferroelectric capacitor formed in a capacitor layer above a semiconductor body; and

a multilayer hydrogen barrier formed above the ferroelectric capacitor, the hydrogen barrier comprising at least one silicon rich silicon oxide layer.

24. The semiconductor device of claim 23, wherein the multilayer hydrogen barrier comprises at least one aluminum oxide layer formed above the ferroelectric capacitor.

25. The semiconductor device of claim 23, wherein the multilayer hydrogen barrier comprises a silicon rich silicon oxide inter-level dielectric formed above the ferroelectric capacitor.

26. The semiconductor device of claim 23, wherein the multilayer hydrogen barrier comprises at least one amorphous silicon layer formed above the ferroelectric capacitor.

27. The semiconductor device of claim 23, wherein the multilayer hydrogen barrier comprises:

an aluminum oxide layer formed over the ferroelectric capacitor; and

a first silicon rich silicon oxide layer formed over the aluminum oxide layer.

28. The semiconductor device of claim 27, wherein the multilayer hydrogen barrier further comprises an amorphous silicon layer formed over the first silicon rich silicon oxide layer and a second silicon rich silicon oxide layer formed over the aluminum oxide layer.